Data-Over-Cable Service Interface Specifications
DCA - MHAv2

Remote DOCSIS Timing Interface

CM-SP-R-DTI-I02-151001

ISSUED

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1 SCOPE

1.1 Introduction and Purpose[1]

This specification is part of a series of specifications that defines modular headend architecture version 2 (MHAv2). Specifically, it outlines a timing protocol between a cable converged access platform core function (CCAP-Core) and one or more remote physical Layer devices (Remote PHY Device or RPD) that enables the RPD to support DOCSIS, Video, and Out-of-Band (OOB) services.

The DOCSIS specification originally envisioned the cable modem termination system core function (CMTS Core), as one entity which integrated the edge-QAM (EQAM) modulators and upstream receiver functions. Therefore, there was no need for external synchronization.

The original MHA architecture was designed to allow the CMTS Core, the upstream receiver, and the EQAM modulator functions to reside in separate boxes, but still physically located close to each other. To make this work, the DOCSIS Timing Interface (DTI) specification was created in order to synchronize the different boxes. In this architecture, a DTI master transported time and phase information to clients via a 10.24 MHz master clock and a 32-bit DOCSIS timestamp.

The MHAv2 architecture extends the concept of MHA by allowing the CCAP Core to be located at greater physical distances from the QAM modulation and demodulation functions. To achieve this, the Remote PHY specification defines the modulation and de-modulation functions to be located together in the Remote PHY Device (RPD). Since the RPD may be located at various different physical locations within the HFC network, it is not practical to distribute the MHA version of DTI to these locations. The MHAv2 version of DTI (i.e., R-DTI) defines how to distribute phase and frequency information from the CCAP Core device to remote PHY devices within the HFC network.

1.2 MHAv2 Interface Documents

A list of the documents in the MHAv2 family of specifications is provided below. For updates, refer to http://www.cablelabs.com/specs/specification-search/.

Table 1 - List of MHAv2 Specifications

Designation	Title
CM-SP-R-PHY	Remote PHY Specification
CM-SP-R-DEPI	Remote Downstream External PHY Interface Specification
CM-SP-R-UEPI	Remote Upstream External PHY Interface Specification
CM-SP-GCP	Generic Control Plane Specification
CM-SP-R-DTI	Remote DOCSIS Timing Interface Specification
CM-SP-R-OOB	Remote Out-of-Band Specification
CM-SP-R-OSSI	Remote PHY OSS Interface Specification

NOTE: MHAv2 does not explicitly use the original DTI specification or any of the original Modular Headend Architecture specifications.

[1] Revised per R-DTI-N-15.1361.3 on 9/20/15 by JB.

1.3 Requirements and Conventions

Throughout this document, the words that are used to define the significance of particular requirements are capitalized. These words are:

"MUST"	This word means that the item is an absolute requirement of this specification.
"MUST NOT"	This phrase means that the item is an absolute prohibition of this specification.
"SHOULD"	This word means that there may exist valid reasons in particular circumstances to ignore this item, but the full implications should be understood and the case carefully weighed before choosing a different course.
"SHOULD NOT"	This phrase means that there may exist valid reasons in particular circumstances when the listed behavior is acceptable or even useful, but the full implications should be understood and the case carefully weighed before implementing any behavior described with this label.
"MAY"	This word means that this item is truly optional. One vendor may choose to include the item because a particular marketplace requires it or because it enhances the product, for example; another vendor may omit the same item.

2 REFERENCES

At the time of publication, the editions indicated were valid. All references are subject to revision, and users of this document are encouraged to investigate the possibility of applying the most recent editions of the documents listed below. References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific. For a nonspecific reference, the latest version applies.

2.1 Normative References

In order to claim compliance with this specification, it is necessary to conform to the following standards and other works as indicated, in addition to the other requirements of this specification. Notwithstanding, intellectual property rights may be required to use or implement such normative references.

[DRFI] Downstream RF Interface Specification, CM-SP-DRFI-I14-131120, November 20, 2013, Cable Television Laboratories, Inc.

[DTI] DOCSIS Timing Interface, CM-SP-DTI-I06-150305, March 5, 2015, Cable Television Laboratories, Inc.

[GCP] Generic Control Plane Specification, CM-SP-GCP-I01-150615, June 15, 2015, Cable Television Laboratories, Inc.

[G.8260] ITU-T Recommendation G.8260, Definitions and terminology for synchronization in packet networks, 2012.

[G.8261] ITU-T Recommendation G.8261, Timing and synchronization aspects in packet networks, 2008.

[MULPIv3.1] DOCSIS MAC and Upper Layer Protocols Interface Specification, CM-SP-MULPIv3.1-I07-150910, September 10, 2015, Cable Television Laboratories, Inc.

[PHYv3.0] DOCSIS 3.0 Physical Layer Specification, CM-SP-PHYv3.0-I12-150305, March 5, 2015, Cable Television Laboratories, Inc.

[PHYv3.1] DOCSIS 3.1 Physical Layer Specification, CM-SP-PHYv3.1-I07-150910, September 10, 2015, Cable Television Laboratories, Inc.

[DOCSIS PHY] Refers to both [PHYv3.0] and [PHYv3.1].

[IEEE 1588] IEEE-1588-2008, Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems, July 2008, http://standards.ieee.org/findstds/standard/1588-2008.html.

[ISO 13818-1] ISO/IEC 13818-1:2013, Information Technology – Generic Coding of Moving Pictures and Associated Audio Information. Part 1: System, May 23, 2013.

[R-DEPI] Remote Downstream External PHY Interface Specification, CM-SP-R-DEPI-I02-151001, October 1, 2015, Cable Television Laboratories, Inc.

[RFIv2.0] DOCSIS Radio Frequency Interface Specification, CM-SP-RFIv2.0-C02-090422, April 22, 2009, Cable Television Laboratories, Inc.

[R-OOB] Remote Out-of-Band Specification, CM-SP-R-OOB-I01-150615, June 15, 2015, Cable Television Laboratories, Inc.

[R-PHY] Remote PHY Specification, CM-SP-R-PHY-I02-151001, October 1, 2015, Cable Television Laboratories, Inc.

[R-UEPI] Remote Upstream External PHY Interface Specification, CM-SP-R-UEPI-I01-150615, June 15, 2015, Cable Television Laboratories, Inc.

[SCTE 55-1] ANSI/SCTE 55-2009, Digital Broadband Delivery System: Out of Band Transport Part 1: Mode A.

[SCTE 55-2] ANSI/SCTE 55-2-2008, Digital Broadband Delivery System: Out of Band Transport Part 2: Mode B.

2.2 Informative References

This specification has the following informative reference.

[IEEE 802.1AS] IEEE-802.1AS-2011, IEEE Standard for Local and Metropolitan Area Networks - Timing and Synchronization for Time-Sensitive Applications in Bridged Local Area Networks, March, 2011.

2.3 Reference Acquisition

- Cable Television Laboratories, Inc., 858 Coal Creek Circle, Louisville, CO 80027; Phone +1-303-661-9100; Fax +1-303-661-9199; http://www.cablelabs.com
- Institute of Electrical and Electronics Engineers (IEEE), +1 800 422 4633 (USA and Canada); http://www.ieee.org
- Internet Engineering Task Force (IETF) Secretariat, 48377 Fremont Blvd., Suite 117, Fremont, California 94538, USA, Phone: +1-510-492-4080, Fax: +1-510-492-4001, http://www.ietf.org
- International Organization for Standardization (ISO), Tel.: +41 22 749 02 22, Fax: +41 22 749 01 55, www.standardsinfo.net
- SCTE, Society of Cable Telecommunications Engineers Inc., 140 Philips Road, Exton, PA 19341 Phone: +1-800-542-5040, Fax: +1-610-363-5898, Internet: http://www.scte.org/

3 TERMS AND DEFINITIONS

This specification uses the following terms:

Cable Modem	A modulator-demodulator at subscriber locations intended for use in conveying data communications on a cable television system.
CCAP-Core	A CCAP device that uses MHAv2 protocols to interconnect to an RPD.
Converged Interconnect Network	The network (generally gigabit Ethernet) that connects a CCAP-Core to an RPD.
Customer Premises Equipment	Equipment at the end user's premises; may be provided by the service provider.
Data Rate	Throughput, data transmitted in units of time usually in bits per second (bps).
Decibels	Ratio of two power levels expressed mathematically as dB = $10\log_{10}(P_{OUT}/P_{IN})$.
Decibel-Millivolt	Unit of RF power expressed in decibels relative to 1 millivolt, where dBmV = $20\log_{10}$(value in mV/1 mV).
Downstream	1. Transmissions from CMTS to CM. This includes transmission from the CMTS Core to the RPD, as well as the RF transmissions from the RPD to the CM. 2. RF spectrum used to transmit signals from a cable operator's headend or hub site to subscriber locations.
Edge QAM modulator	A headend or hub device that receives packets of digital video or data. It re-packetizes the video or data into an MPEG transport stream and digitally modulates the digital transport stream onto a downstream RF carrier using quadrature amplitude modulation (QAM).
Flow	A stream of packets in [R-DEPI] used to transport data of a certain priority from the CMTS Core to a particular QAM channel of the RPD. In PSP operation, there can exist several flows per QAM channel.
Gbps	Gigabits per second
Gigahertz	A unit of frequency; 1,000,000,000 or 10^9 Hz.
GigE	Gigabit Ethernet (1 Gbps)
Hertz	A unit of frequency; formerly cycles per second.
Hybrid Fiber/Coax System	A broadband bidirectional shared-media transmission system using optical fiber trunks between the head-end and the fiber nodes, and coaxial cable distribution from the fiber nodes to the customer locations.
Institute of Electrical and Electronic Engineers	A voluntary organization which, among other things, sponsors standards committees and is accredited by the American National Standards Institute (ANSI).
Internet Engineering Task Force	A body responsible for, among other things, developing standards used in the Internet.
Internet Protocol	An Internet network-layer protocol
kilohertz	Unit of frequency; 1,000 or 10^3 Hz; formerly kilocycles per second
MAC Domain	A grouping of layer 2 devices that can communicate with each other without using bridging or routing. In DOCSIS is the group of CMs that are using upstream and downstream channels linked together through a MAC forwarding entity.
Maximum Transmission Unit	Maximum size of the layer 3 payload of a layer 2 frame.

Mbps	Megabits per second
Media Access Control	Used to refer to the Layer 2 element of the system which would include DOCSIS framing and signaling.
Megahertz	A unit of frequency; 1,000,000 or 10^6 Hz; formerly megacycles per second
Microsecond	10^{-6} second
Millisecond	10^{-3} second
Modulation Error Ratio	The ratio of the average symbol power to average error power.
Multiple System Operator	A corporate entity that owns and/or operates more than one cable system.
Nanosecond	10^{-9} second
Physical Media Dependent Sublayer	A sublayer of the Physical layer which is concerned with transmitting bits or groups of bits over particular types of transmission link between open systems and which entails electrical, mechanical, and handshaking procedures.
QAM channel	Analog RF channel that uses quadrature amplitude modulation (QAM) to convey information
Quadrature Amplitude Modulation	A modulation technique in which an analog signal's amplitude and phase vary to convey information, such as digital data.
Radio Frequency	In cable television systems, this refers to electromagnetic signals in the range 5 to 1000 MHz.
Radio Frequency Interface	Term encompassing the downstream and the upstream radio frequency interfaces.
Remote PHY Device	The Remote PHY Device (RPD) is a device in the network that implements the Remote-PHY/MHAv2 specifications to provide conversion from digital Ethernet transport to analog RF transport.
Timebase	The clock from which all other internally generated clocks and timebases on the device are derived
Upconverter	A device used to change the frequency range of an analog signal, usually converting from a local oscillator frequency to an RF transmission frequency.
Upstream	1. Transmissions from CM to CMTS. This includes transmission from the RPD to the CMTS Core as well as the RF transmissions from the CM to the RPD. 2. RF spectrum used to transmit signals from a subscriber location to a cable operator's headend or hub site.
Upstream Channel Descriptor	The MAC Management Message used to communicate the characteristics of the upstream physical layer to the cable modems.

4 ABBREVIATIONS AND ACRONYMS

This specification uses the following abbreviations:

µs	Microsecond
ATP	Acceptance test plan
BC	Boundary clock
CBR	Constant bit rate
CCAP™	Converged cable access platform
CIN	Converged interconnect network
CLK	Clock
CM	Cable modem
CMCI	Cable modem CPE interface
CMTS	Cable modem termination system
CPE	Customer premises equipment
dB	Decibel
dBc	Decibel carrier
dBmV	Decibel millivolt
DCA	Distributed CCAP Architecture
DEPI	Downstream External-PHY Interface Specification
DLM	DEPI latency measurement
DOCSIS	Data-Over-Cable Service Interface Specifications
DRFI	[DOCSIS] Downstream Radio Frequency Interface (specification)
DS	Downstream
DTI	DOCSIS Timing Interface (specification)
DTP	DOCSIS timing protocol
EEC	Ethernet equipment clock
EQAM	Edge-QAM (modulator)
FEC	Forward error correction
FFO	Fractional frequency offset
FIFO	First in first out
FTP	File transfer protocol
GCP	Generic control plane
GE or GigE	Gigabit Ethernet (1 Gbps)
GHz	Gigahertz
GM	Grandmaster
GPS	Global Positioning System
HA	High availability
HFC	Hybrid fiber/coax
HRM	Hypothetical reference model
HTTP	Hypertext transfer protocol
Hz	Hertz

IEEE	Institute of Electrical and Electronics Engineers
IETF	Internet Engineering Task Force
IP	Internet protocol
IPv4	Internet protocol version 4
IPv6	Internet protocol version 6
ITU	International Telecommunication Union
ITU-T	ITU Telecommunication Standardization Sector
kHz	Kilohertz
log	Logarithm
MAC	Media access control
MAP	Upstream Bandwidth Allocation Map (referred to only as MAP)
MER	Modulation Error Ratio
MHAv2	Modular Headend Architecture Version 2
MHz	Megahertz
MPEG	Moving Picture Experts Group
MPEG-TS	MPEG transport stream
MPT	MPEG-TS payload type
MPTS	Multi program transport stream
ms	Millisecond
MSO	Multiple system operator
MTIE	Maximum time interval error
MTU	Maximum Transmission Unit
NDF	Narrowband digital forward
NDR	Narrowband digital return
ns	Nanosecond
NSI	Network side interface
NTP	Network time protocol
OOB	Out of Band
OC	Ordinary clock
OFDM	Orthogonal frequency division multiplexing
OSSI	Operations System Support Interface
PCR	Program clock reference
PDV	Packet delay variation
PHY	Physical layer
PLC	PHY link channel
PMD	Physical Media Dependent Sublayer
PPB	Parts per billion
PPM	Parts per million
PRC	Primary reference clock
PTP	Precision time protocol
QAM	Quadrature amplitude modulation

QAM ch	QAM Channel
R-DTI	Remote DOCSIS Timing Interface (specification)
RPD	Remote PHY Device
RF	Radio frequency
REQ	Request
RFI	Radio frequency interface
RMS	Root mean square
RNG-RSP	Ranging response
RX	Receiver
SyncE	Synchronous Ethernet
STC	System timing clock
TAI	International Atomic Time
TC	Transparent clock
TCP	Transmission control protocol
TDM	Time division multiplexing
TDMA	Time division multiple access
ToD	Time of day
TS	Timestamp
TSMB	Timestamp message block
TWTT	Two-way time transfer
UCD	Upstream Channel Descriptor
UEPI	Upstream external PHY interface
µs	Microsecond
US	Upstream
UTC	Coordinated Universal Time

5 OVERVIEW

5.1 Introduction[2]

The requirements for timing and synchronization of the MHAv2 architecture come from the following areas.

- Existing DOCSIS specification requirements
- Remote PHY system requirements
- Implementation requirements
- Precision timing services like T-services and wireless backhaul

These requirements place definitions and constraints on the use of the DOCSIS master clock and the DOCSIS timestamp.

As shown in Figure 1, in the MHAv2 architecture, the CMTS Core and the RPD are two entities located in separate chassis, and potentially in different physical locations. The DS PHY and US PHY are located in one assembly—the Remote PHY Device—controlled with a common clock. The upstream scheduler/MAP builder is part of media access control (MAC), and is located at the CMTS Core. The DOCSIS time described by the MAP needs to allow correct burst reception at the RPD. Therefore the CMTS Core and the RPD need to have a common knowledge of the DOCSIS time. Without any synchronization method, the CMTS Core and the RPD run on separate timing domains based on their own local clocks. There will be an offset between CMTS Core DOCSIS timestamp and the RPD DOCSIS timestamp. This offset is not constant but increases or decreases over time because of the drift accumulation caused by the frequency accuracy difference of the two local clocks.

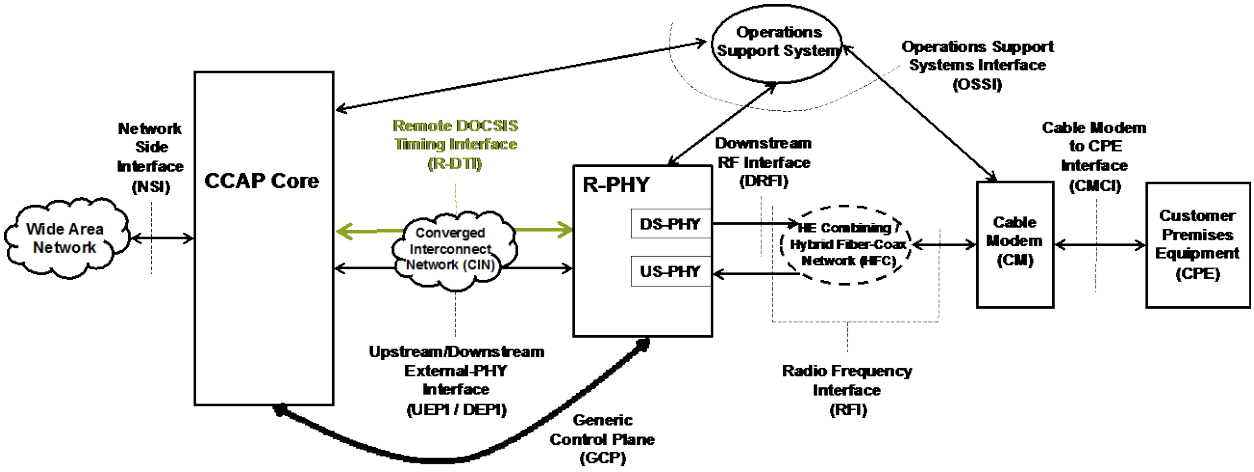

Figure 1 - MHAv2 Reference Architecture for Remote PHY

Similar challenges exist for video and OOB services. The Remote DOCSIS Timing Interface (R-DTI) protocol defined in this document supports the basic synchronization between the CCAP-Core and RPD for DOCSIS/video/OOB services and the precision time synchronization for emerging services such as wireless backhaul.

[2] Revised per R-DTI-N-15.1361.3 on 9/20/15 by JB.

5.2 R-DTI Architecture[3]

5.2.1 Timing Distribution

The method of distributing phase and frequency information depends upon the network between CCAP Core and the RPD devices. While the Remote PHY specifications define Ethernet as the MAC layer protocol, the physical layer may either be traditional full duplex Ethernet or 10G EPON. Furthermore, for traditional Ethernet networks, there may be a routed or switched network between the CCAP Core and the RPDs.

5.2.1.1 Ethernet Timing

For Ethernet based networks, IEEE 1588 allows both phase and frequency information to be transferred between nodes across an existing packet network with switches or routers, thus making it ideal for R-DTI.

IEEE 1588 uses the PTP protocol to communicate timestamp information across a network. By periodically sending timestamp updates across the network between a master device and a slave device, the slave device can determine both the phase and frequency. In order to reduce any phase offset introduced by latencies through the network, IEEE 1588 defines a protocol for calculating the latency across sections of the network, and then compensating for those latencies. The latency calculations assume that the link is symmetric, and therefore the protocol works well for traditional full duplex Ethernet networks. IEEE 1588 also defines a protocol for determining the latency through any intervening switches or routers within the network, but the device must be IEEE 1588 capable. If the devices are not IEEE 1588 capable, the phase offsets and convergence times within the network will be greater.

Since [IEEE 1588] already provides detailed protocol information, only the most relevant and basic information is listed here (see Section 5.3). For additional detailed information, please refer to [IEEE 1588] directly.

5.2.1.2 10G EPON Timing

10G Symmetrical or Asymmetrical EPON networks may also be used to connect the CCAP-Core to the RPD devices. In this configuration, the CCAP Core is the EPON OLT, and the RPD contains an EPON ONU.

The usage of IEEE 1588 across asymmetrical links, such as EPON, is problematic since 1588 relies on the basic premise that the link delays are symmetrical. In order to address this issue for EPON links, the [IEEE 802.1AS] specification included Clause 13 in order to define a standard method for transferring time and frequency information across an EPON link. In this scenario IEEE 1588 Timing is terminated at the CCAP Core and the [IEEE 802.1AS] protocol is used to transfer timing from the CCAP Core to the ONU in the RPD, as shown in Figure 2 below.

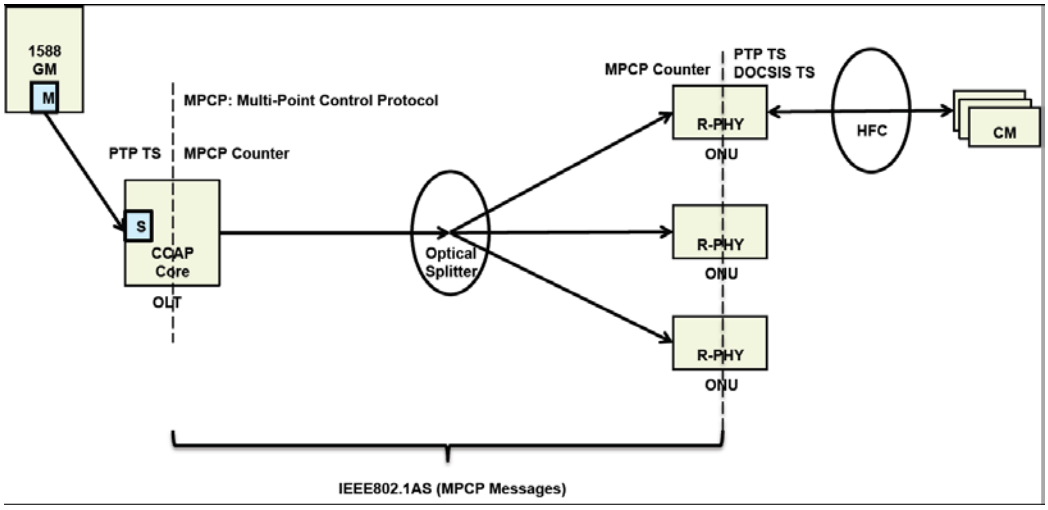

Figure 2 - [IEEE 802.1AS] Deployment Scenario

[3] Revised per R-DTI-N-15.1361.3 on 9/20/15 by JB.

In the upstream direction, the operation of EPON is analogous to DOCSIS. Multiple ONU devices share the EPON upstream link, and take turns bursting on the upstream in a TDM fashion. Much like DOCSIS, EPON has its own timestamp (the MPCP timer) and its own ranging protocol to align the ONU devices. The [IEEE 802.1AS] specification takes advantage of these facilities in order to provide the best possible delay estimate to the ONU. The actual EPON timer facility is defined to be a 32-bit timer with a resolution of 16ns. Therefore, the timer rolls over about every 68.7 seconds. 802.1 as defines a method of transferring 1588 ToD information such that the lower bits of the ToD are referenced to the MPCP timer. Using this method allows the 1588 ToD to be transferred from the OLT to the ONU with about 100ns accuracy (or better).

EPON obtains its frequency synchronization from the downstream symbol clock, much like Synchronous Ethernet. Therefore, as long as the OLT device operates from a clock which is referenced to a 1588 source, the ONU device will remain synchronized.

Since an EPON network establishes the OLT (i.e., CCAP Core) as the timing master, R-DTI Node Master mode is not supported when using an EPON network.

5.2.1.3 Timestamp Conversion

While the defined timestamp counters for [IEEE 1588] (PTP timestamp) and 10G EPON (MPCP timer) increment at the same basic rate, the DOCSIS timestamp increments at a different rate. Since R-DTI needs to transfer the DOCSIS timestamp from the master device to slave devices, a translation to the IEEE 1588 format is required to send the timestamp/phase information across the network.

In order to accomplish this, DOCSIS 3.1 has added additional bits to the DOCSIS 3.0 timestamp, and has defined an all zero value to correlate to an internal atomic time value (TAI) of 00:00:00 on January 1st, 1970. This was done to match the pre-existing definition of the PTP timestamp defined by IEEE 1588. Therefore, any given DOCSIS 3.1 timestamp value can be translated to an equivalent IEEE 1588 timestamp value. This is critical for allowing precise DOCSIS phase information to be transferred across an IEEE 1588 or 10G EPON network.

For a 10G EPON network, the CCAP Core must synchronize the MPCP timer to be phase aligned with a IEEE 1588 timer maintained by the CCAP Core. Since the MPCP timer is only 32-bits wide, the upper bits of the IEEE 1588 timestamp value must be communicated over the packet network from the CCAP Core to the RPDs. The RPD may then combine the upper bits with the MPCP timer to form an accurate IEEE 1588 PTP timestamp. The PTP timestamp may then be translated to a DOCSIS 3.1 timestamp value.

For non-3.1 DOCSIS devices, the DOCSIS 3.1 timestamp is easily translated to a 32-bit DOCSIS timestamp value by extracting 32-bits starting from the 10.24MHz bit (i.e., bit 9) of the DOCSIS 3.1 timestamp as shown in Figure 3.

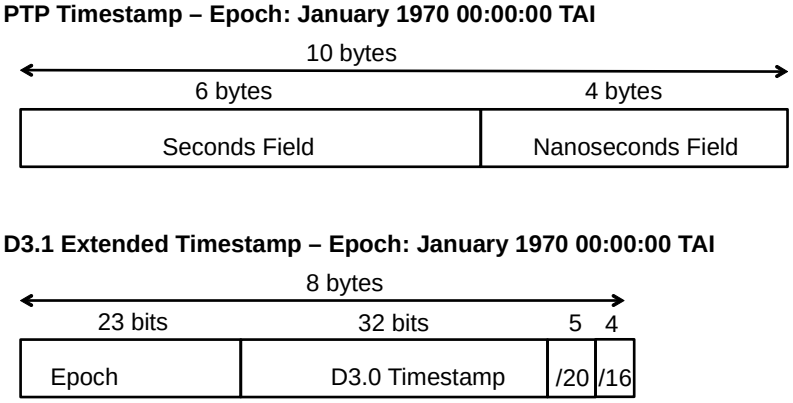

Figure 3 - PTP Timestamp, DOCSIS 3.0 Timestamp and DOCSIS 3.1 Extended Timestamp

5.2.2 Timing Master Requirements

In an R-DTI system, a single timing master distributes phase and frequency information to the other devices located in the same timing domain. The timing master can be provided by the CCAP Core or an external GM.

The R-DTI master MUST comply with the following DOCSIS [DRFI] requirements for timing accuracy and drift:

- Section 6.3.5.2, CMTS or EQAM Master Clock Jitter for Asynchronous Operation
- Section 6.3.5.3, CMTS or EQAM Master Clock Jitter for Synchronous Operation
- Section 6.3.5.4 CMTS or EQAM Master Clock Frequency Drift for Synchronous Operation

Systems implementing physical layer modulation and demodulation functionality need to adhere to additional timing specifications as per [DRFI].

The timing master may derive its timing from any number of external sources as long as the specified [DRFI] timing requirements are met.

5.2.3 Timing Slave Requirements

Typically, the RPD is the timing slave, but for Ethernet/IEEE 1588 systems, the CCAP Core may also be implemented as a timing slave. For 10G EPON based systems, the CCAP Core MAY NOT be a timing slave.

A timing slave device derives both phase and frequency information from the timing master. Phase information is sent to the timing slave as a timestamp within a packet. Algorithms defined in the IEEE 1588 specification (or the 10G EPON specification) are then used to calculate round trip delay times in order to minimize the phase difference between the master and the slave. Furthermore, hardware is typically used to timestamp packets as they depart and/or arrive in order to provide improved accuracy when measuring latency.

Once phase information is obtained, the timing slave must achieve frequency lock to the timing master. In the case of IEEE 1588, frequency lock is obtained by receiving a number of timestamp updates, and processing the timestamp values through a low pass filter algorithm in order to determine the frequency of the timing master. If the timing slave provides clocks to integrated DOCSIS modulators and demodulators, the timing slave MUST adjust its clock gradually to bring the slave's timestamp back into phase alignment with the master. The rate of adjustment MUST be less than or equal to 1e-8 per second, as specified by the DOCSIS CMTS drift requirements for synchronous operation.

If the CCAP Core is the timing slave and RPD is the master, the CCAP Core MAY maintain phase lock by discretely adjusting a local DOCSIS timestamp. In such a scheme, the CCAP Core MUST maintain separate DOCSIS timestamps for every RPD.

In a 10G EPON system, the RPD recovers the frequency by locking onto the downstream EPON symbol clock. In this scheme, the local DOCSIS clock MUST be synthesized from the recovered EPON clock.

The RPD MAY use synchronous Ethernet to recover the frequency from the Ethernet symbol clock if a synchronous Ethernet network is maintained between the CCAP Core and the RPD. In this scheme, the local DOCSIS clock MUST be synthesized from the recovered Ethernet clock.

5.3 IEEE 1588 Operation[4]

5.3.1 IEEE 1588 Utilization

[IEEE 1588] provides time synchronization between two nodes across a packet network without mandating all intermediate nodes being replaced, hence becomes the best tool for the R-DTI implementation. [IEEE 1588] standardizes the PTP and the node, system and communication properties necessary to support PTP. Only the most relevant and basic information is listed here. For the detailed information, please refer to [IEEE 1588] directly.

[4] Revised per R-DTI-N-15.1361.3 on 9/20/15 by JB.

5.3.2 PTP Devices

A Precision Time Protocol (PTP) system is a distributed, networked system consisting of a combination of PTP and non-PTP devices. PTP devices include ordinary clocks (OC), boundary clocks (BC), end-to-end transparent clocks (TC), peer-to-peer transparent clocks, and management nodes. Non-PTP devices include bridges, routers, and other infrastructure devices that do not generate, modify, or consume PTP messages.

The PTP devices that are most relevant to R-DTI are OCs and BCs.

5.3.2.1 Ordinary Clock

An ordinary clock (OC) communicates with the network via two logical interfaces based on a single physical port. The event interface is used to send and receive event messages, which are timestamped by the timestamp generation block based on the value of the local clock. The general interface is used to send and receive general messages. An OC in a domain supports a single copy of the protocol and has a single PTP state. The OC can be the GM clock in a system, or it can be a slave clock in a master-slave hierarchy. It contains a protocol engine and has the following functions:

- Sends and receives PTP messages
- Maintains the data sets
- Executes the state machine associated with the port
- If the port is in the slave state (synchronized to a master), it computes the master's time based on the received PTP timing messages and timestamps that were generated.

The control loop in the local clock adjusts the clock to agree with the time of its master if the OC port is in the slave state. If the port is in the master state, the local clock is free running or possibly synchronized to an external source of time such as GPS. If the port is in the master state and the OC is the GM clock of the domain, then the local clock is typically synchronized to an external source of time traceable to International Atomic Time (TAI) and Coordinated Universal Time (UTC), such as a GPS-based system.

5.3.2.2 Boundary Clock

The boundary clock (BC) typically has several physical ports with each physical port communicating with the network via two logical interfaces: event and general. Each port of a BC is like the port of an OC, with the following exceptions:

1. The clock data sets are common to all ports of the BC.
2. The local clock is common to all ports of the BC.
3. Each protocol engine has the additional function of resolving the states of all ports to determine which port provides the time signal used to synchronize the local clock.

5.3.3 PTP Messages

The PTP defines event and general PTP messages. Event messages are timed messages in that an accurate timestamp is generated at both transmission and receipt. General messages do not require accurate timestamps. The set of event messages consists of:

- Sync
- Delay_Req
- Pdelay_Req
- Pdelay_Resp

The set of general messages consists of:

- Announce
- Follow_Up

- Delay_Resp
- Pdelay_Resp_Follow_Up
- Management
- Signaling

Among these messages, the Sync, Delay_Req, Follow_Up, and Delay_Resp messages are used to generate and communicate the timing information needed to synchronize ordinary and boundary clocks using the delay request-response mechanism.

Figure 4 illustrates the basic synchronization message exchange. The messages exchange pattern is as follows:

1. The master sends a Sync message to the slave and notes the time *t1* at which it was sent.
2. The slave receives the Sync message and notes the time of reception *t2*.
3. The master conveys to the slave the timestamp *t1* by:

   a. Embedding the timestamp *t1* in the Sync message. This requires some sort of hardware processing for highest accuracy and precision.

   b. Embedding the timestamp *t1* in a Follow_Up message.
4. The slave sends a Delay_Req message to the master and notes the time of delivery *t3*.
5. The master conveys to the slave the timestamp *t4* by embedding it in a Delay_Resp message.

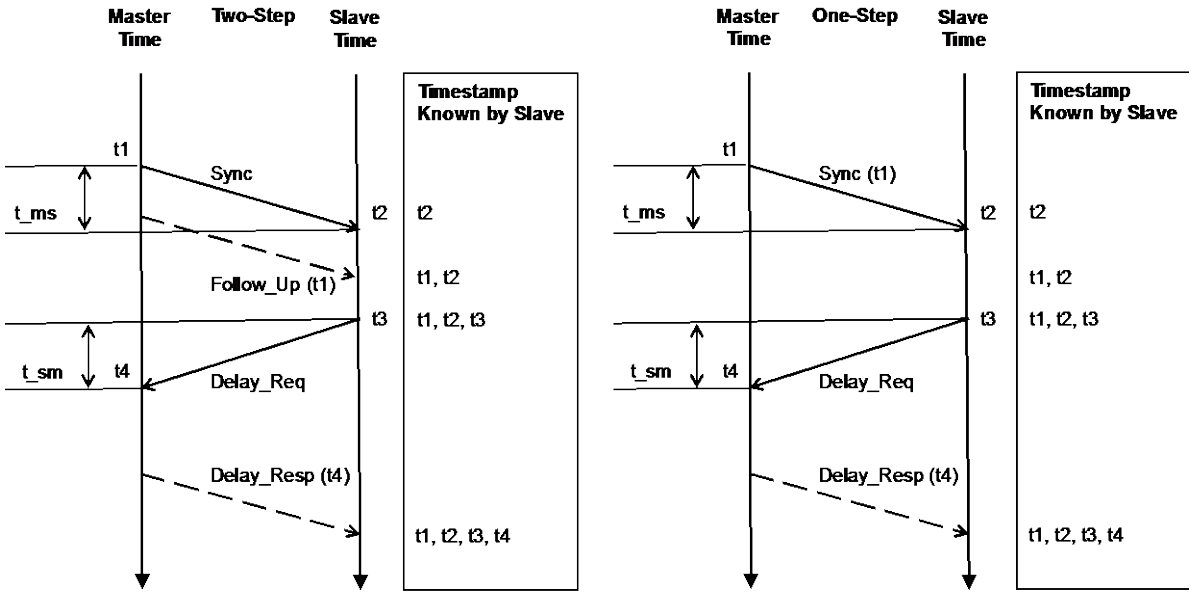

Figure 4 - PTP Basic Synchronization Message Exchange

At the conclusion of this exchange of messages, the slave possesses all four timestamps. These timestamps may be used to compute the offset of the slave's clock with respect to the master and the mean propagation time of messages between the two clocks.

The computation of offset and propagation time assumes that the master-to-slave and slave-to-master propagation times are equal. Any asymmetry in propagation time introduces an error in the computed value of the clock offset. The computed mean propagation time differs from the actual propagation times due to the asymmetry.

The details of all the messages are described in [IEEE 1588].

5.3.4 Achieving Frequency Synchronization

Without frequency synchronization, the master and slave clocks will drift apart between message updates. Because the sync messages are sent repetitively, the slave is able to calculate the drift between the master clock and slave clock with the following formula

$$Drift = \frac{\Delta t2(m,n) - \Delta t1(m,n)}{\Delta t1(m,n)}$$

$\Delta t1(m,n)$ is the original timestamp difference (@master) of the two Sync messages with multiple Sync messages in between, and $\Delta t2(m,n)$ is the arrival timestamp (@slave) difference of the two Sync messages. By comparing the drift over time, the slave can synthesize a frequency that is synchronized to the master clock.

Frequency recovery is only required if alternate frequency traceability methods, such as Synchronous Ethernet, do not exist and high levels of time accuracy are required. If Layer 1 frequency synchronization is available, it should be used since it provides a higher level of frequency accuracy and stability.

5.3.5 Achieving Time Synchronization

Once frequency synchronization is achieved, the slave clock can maintain a constant phase relationship to the master clock; then the delay request-response mechanism is used to measure the <meanPathDelay> between the master and clock. PTP assumes that the delays from the master to the slave and from the slave to the master are perfectly symmetrical, allowing the meanPathDelay to be calculated using the following formula:

$$< meanPathDelay > = \frac{[(t2 - t1) + (t4 - t3)]}{2} = \frac{[t2 - t3] + (t4 - t1)]}{2}$$

The value of the slave time on the next *t2* time is calculated with:

$$Tslave\ @\ t2 = t1 + < meanPathDelay >$$

Time recovery can require a very complex algorithm that is affected by many real world effects such as slight variations in frequency, packet delay variation (PDV), and network asymmetry.

5.3.5.1 Time Synchronization Error Sources

There are three main sources of error for time synchronization in any two-way time transfer (TWTT) protocol including PTP. These are described in the following subsections.

5.3.5.1.1 Fixed Path Asymmetry

Because PTP assumes that the master-to-slave (t_{ms}) and slave-to-master (t_{sm}) paths are perfectly symmetrical, any asymmetry in the paths will result in a time offset between the master and slave nodes equal to the following basic formula:

$$t\_error = \frac{t\_ms - t\_sm}{2}$$

The asymmetry can arise from many sources, including but not limited to:

- Network topology differences;
- Timestamp location differences within the master, slave, or transparent clock nodes;
- Node delay variations through nonparticipant nodes.

5.3.5.1.2 Packet Delay Variation (PDV)

Because time synchronization relies on constant flight time between the master and slave, any variability in packet delivery in either direction will make it more difficult for the slave to accurately recover time and frequency. Each calculation of drift, offset and one-way delay will produce unique results based on the PDV in the network.

Therefore, slaves use a slave servo algorithm to integrate the results to determine the true offset and one-way delay measurements over time. Alternatively a slave servo algorithm could pre-process the time values before calculating the offset drift and one-way delay, looking for minimum packet delays.

The algorithm is not standardized as part of [IEEE 1588].

5.3.5.1.3 Frequency Drift Between Master and Slave

In between time updates from the slave servo algorithm, PTP time is advancing based on the slave's holdover frequency. If the frequency at the master and the slave are not perfectly synchronized, the time at the slave will drift away from the master time. The rate of drift is proportional to the frequency difference.

If the frequency on the slave is recovered from the packet timing flow, as with PTP, then the accuracy of the frequency recovery will be impacted by the PDV through the network.

5.4 R-DTI Deployment Scenarios for DOCSIS[5]

5.4.1 Node_Slave

Figure 5 shows frequency and phase distribution between the CMTS Core and the RPD with the RPD being the timing slave.

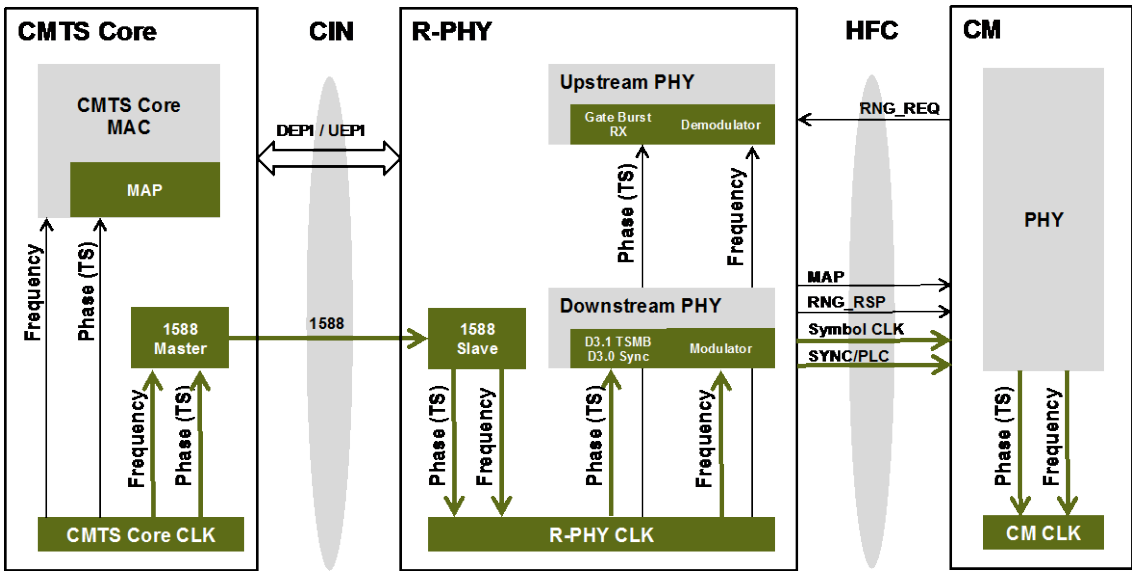

Figure 5 - R-DTI Node_Slave Architecture – RPD Slave / Core Master

The Node_Slave mode is a typical 1588/PTP application, and the key element of this architecture is to have a single clock domain system; both frequency and phase of the RPD and the CMTS Core are synchronized. One way to achieve this goal is to make the CMTS Core the 1588 master and the RPD the 1588 slave as shown in Figure 5. Alternatively, they can both be 1588 slaves and synchronize to a 1588 GM in a single 1588 clock domain, as shown in Figure 6. In this architecture, the synchronization mode is linked with the DOCSIS operation mode. The CMTS Core and the RPD have to be in the same PTP clock domain.

[5] Revised per R-DTI-N-15.1361.3 on 9/20/15 by JB.

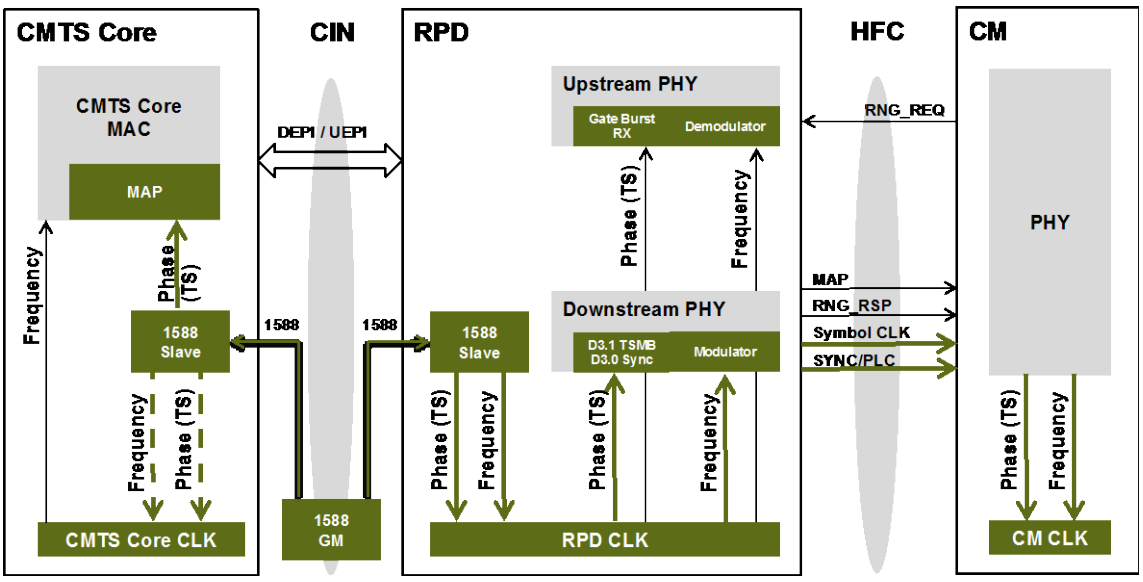

Figure 6 - R-DTI Node_Slave Architecture – RPD Slave / Core Slave / Common Master

Figure 7 shows the basic synchronization message exchange in the R-DTI Node_Slave architecture. Refer to Section 5.3.4 and Section 5.3.5 for information on achieving frequency and time synchronization using PTP messages.

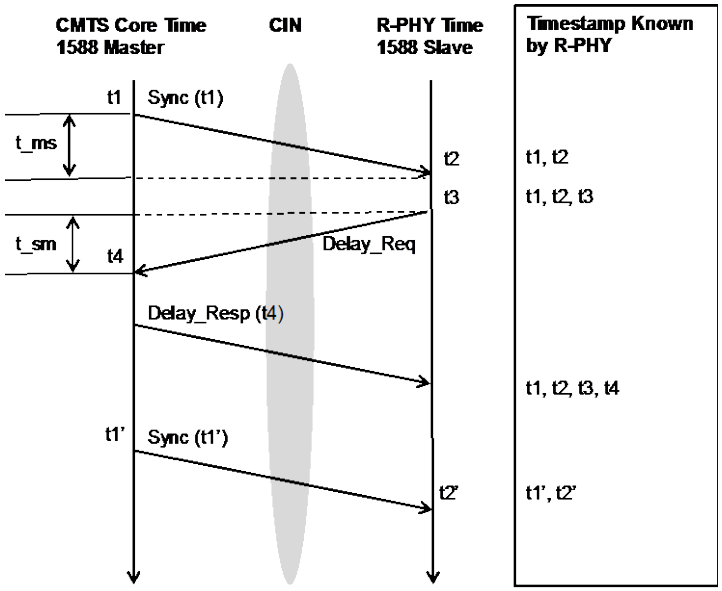

Figure 7 - Basic Synchronization Message Exchange in Node_Slave Mode

5.4.1.1 Performance Considerations

In Node_Slave mode, both the DOCSIS master clock frequency and the DOCSIS timestamp are driven by the PTP source, and MUST meet all applicable [DRFI] and [DOCSIS PHY] requirements.

The phase/time accuracy of the synchronization impacts the Request_Grant round trip delay and MAP advance calculation. The synchronization error needs to be considered as part of engineering margin for MAP advance calculation as described in Appendix I, RPD and DOCSIS System Performance.

The timestamp error between the CMTS Core and the RPD depends on many factors including—but not limited to—the following:

- The timestamp mechanism. The timestamp shall be performed as close as possible to the physical interface to minimize the PDV inside the devices.
- The CIN characteristic. The performance is impacted by the path asymmetry and the PDV in the network.
- Algorithms at the RPD. In order to minimize the impact from the packet network using PTP packets, specific algorithms may need to be implemented at the RPD to guarantee frequency and phase performance.

5.4.1.2 DLM Utilization

In the Node_Slave operation mode, full time synchronization can be achieved and the DEPI latency measurement (DLM) protocol specified in Remote Downstream External PHY Interface [R-DEPI] specification can be utilized to measure the CIN delay. The DLM is important because it prevents overestimating and/or underestimating the network delay effect, and therefore improves efficiency without compromising reliability. It is important to recognize that PTP is not an alternative to DLM for these reasons:

- Only PTP slaves, but not masters, are aware of all timestamps required for the latency measurement. In DOCSIS, CMTS Core needs to obtain the latency information to calculate MAP advance, and as PTP master it does not have enough information to do so. DLM, on the other hand, makes the timestamp information available to the master.
- DLM offers different reference points regarding timestamp compared to PTP.

5.4.2 Node_Master

Figure 8 shows frequency and phase distribution between the CMTS Core and the RPD with the RPD being the timing master.

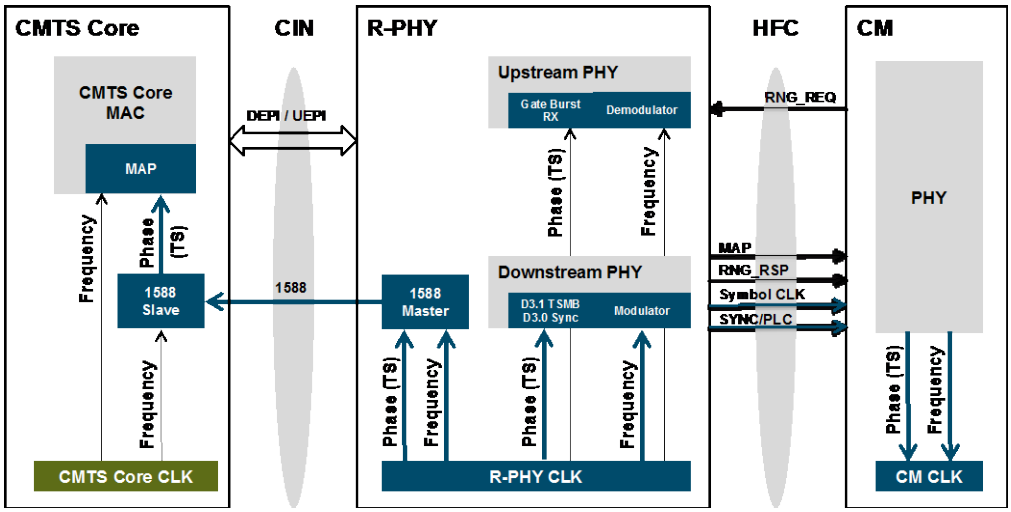

Figure 8 - R-DTI Node_Master Architecture – RPD as the Timing Master

In the Node_Master architecture, the RPD acts as a 1588 Master, while CMTS Core acts as a 1588 Slave.

The RPD distributes its frequency and phase information through PTP. CMTS Core MAC obtains the frequency and phase information from the timestamp messages and runs a phase calibration process to track the RPD time without achieving frequency synchronization.

The CMTS Core MAC timestamp is still driven by the CMTS Core system clock frequency, however the new timestamp values recovered from the RPD PTP messages are loaded periodically, so the MAC timestamp gets

corrected before it drifts too far away from the RPD timestamp. To give an example, if the CMTS Core local clock frequency accuracy is +5 parts per million (PPM), and the RPD clock frequency accuracy is -5PPM, and the update frequency is set to once per second, then the CMTS Core MAC timestamp will be 10 µs ahead of the RPD timestamp at the end of that 1 second interval even if they were perfectly aligned at the beginning of the interval. They will be aligned again when another update occurs.

The RPDs can be on different clock domains—for example, each running on its own oscillator—so the CMTS Core needs to track each individual RPD clock domain separately. The CMTS Core becomes an ordinary clock (slave) in each 1588 clock domain, but it may participate in hundreds or even thousands of 1588 clock domains at the same time.

The RPD may be in a free run mode with its frequency driven from an internal frequency source such as an oscillator, and its time driven from a time protocol such as NTP. Or it may synchronize to a 1588 GM in the packet network for both frequency and time. In the latter case, the RPD is a 1588 BC instead of OC—it is a slave clock to the 1588 GM in the network and a master clock to the CCAP-Core. Similarly, the CMTS Core may be in a free run mode or synchronized to an external source.

NOTE: The synchronization modes of either or both entities (CMTS Core or RPD) do not impact the DOCSIS operation when the Node_Master mode is chosen.

5.4.2.1 Synchronization Message Exchange

Figure 9 shows the basic synchronization message exchange in the R-DTI Node_Master architecture. Refer to Section 5.3.4 and Section 5.3.5 on achieving frequency and time synchronization using PTP messages. Although the physical frequency of the CMTS Core is not synchronized to the RPD clock, the drift information may be used to better estimate the time.

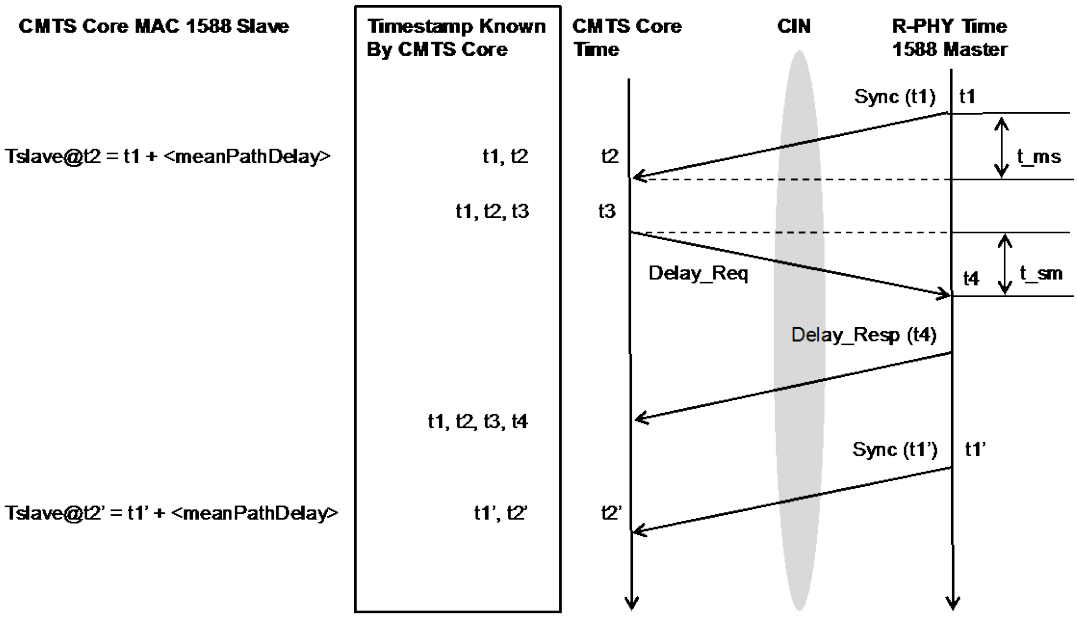

Figure 9 - Basic Synchronization Message Exchange in Node_Master Mode

5.4.2.2 Performance Consideration

There is no actual physical frequency synchronization in this architecture (Node_Master mode); therefore frequency stability is less of a concern.

Similarly to the Node_Slave mode, the accuracy of the synchronization impacts the Request_Grant round trip delay and MAP advance calculation. The synchronization accuracy can be affected by many factors such as timestamp mechanism, network topology, traffic behavior, client algorithms, etc.

Since the physical frequency between the two entities is not in sync in this mode, the drift accumulation due to the frequency offset of the two between the updates could contribute to additional phase error compared to the Node_Slave mode.

5.4.2.3 High Availability Consideration

Mixed Node_Master and Node_Slave

The operation modes described in Section 5.4.1 and Section 5.4.2 can co-exist in a single CMTS system. The example is shown in Figure 10. Each color represents one 1588 clock domain.

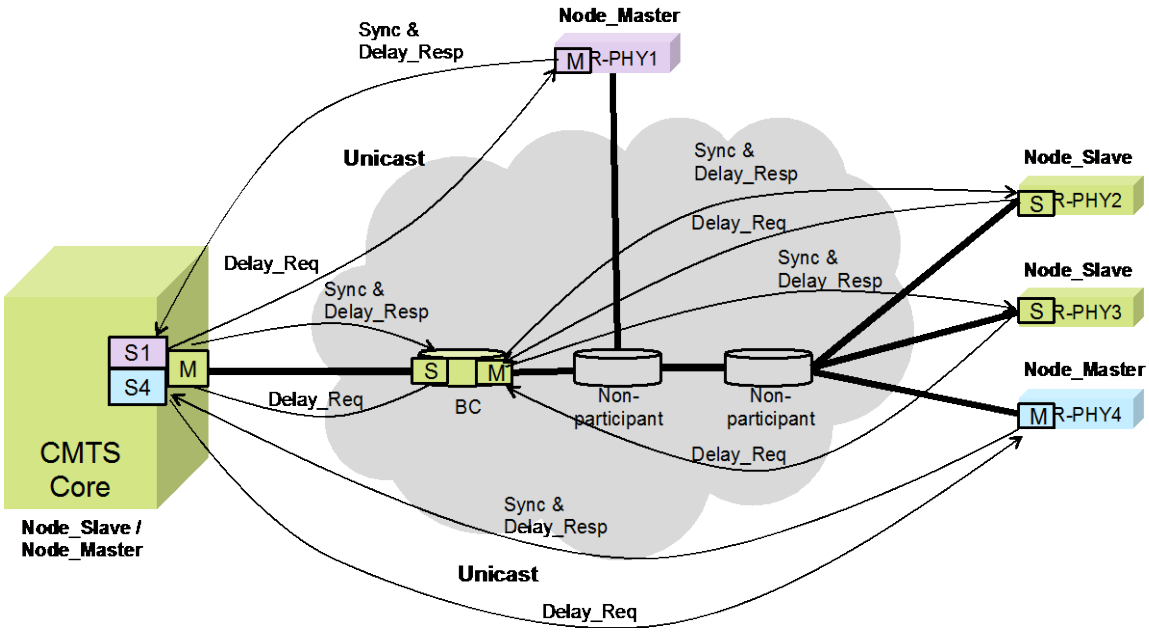

Figure 10 - Operation Modes Co-existing in a Single CMTS System

The RPDs R-PHY2 and R-PHY3 (shown in light green in Figure 10) operate as 1588 slaves and synchronize to a 1588 master clock—the BC node in the network, and the BC node synchronizes to the CMTS Core. The CMTS Core acts as the 1588 grandmaster clock of this 1588 clock domain. The DOCSIS operation mode between CMTS Core and RPDs R-PHY2 and R-PHY3 is Node_Slave mode.

At the same time, the CMTS Core is a 1588 slave clock to RPD R-PHY1, and also a 1588 slave clock to RPD R-PHY4. The DOCSIS operation mode between CMTS Core and RPDs R-PHY1 and R-PHY4 is Node_Master mode.

There are three independent clock domains in Figure 10. The 1588 protocol between CMTS Core and RPD R-PHY1 is established in a unicast model so the BC nodes between the two can forward the message accordingly. A unicast model SHALL be considered for all Node_Master operations unless the 1588-aware nodes in the CIN can be configured as 1588 Transparent Clocks.

5.4.2.4 DOCSIS Operation with Multiple CMTS Cores

Figure 11 shows the deployment example with multiple CMTS Cores. Each color represents one 1588 clock domain.

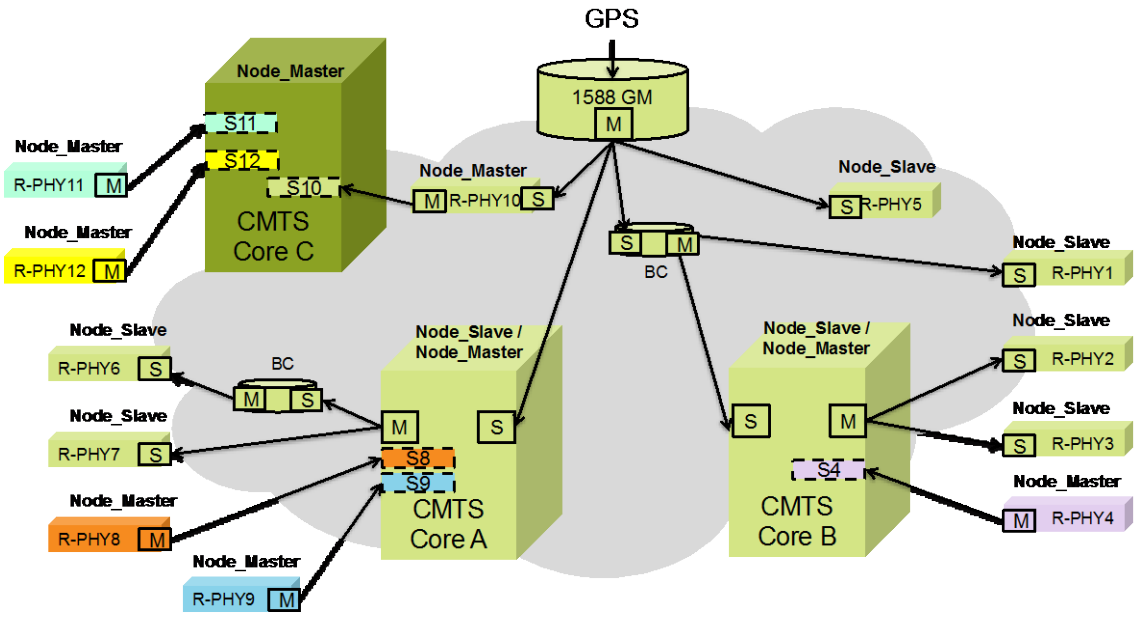

Figure 11 - Deployment Example with Multiple CMTS Cores

CMTS Core A and CMTS Core B are in the same 1588 clock domain, therefore all the RPDs that operate in Node_Slave mode to these two Cores are in the same clock domain. If CMTS Core A goes down, and the RPDs R-PHY6/7 are routed to CMTS Core B instead, the synchronization between the RPDs R-PHY6/7 and CMTS Core B is established already, and theoretically it takes less time to resume the services. In reality, the service recovery time will depend on many factors.

The CMTS Core C is not part of the same 1588 clock domain. It may not have a qualified DOCSIS master clock, but RPDs R-PHY10/11/12 can operate with CMTS Core C by operating in Node_Master mode. At the same time, RPD R-PHY10 can offer precision timing services by synchronizing to the other 1588 clock domain with traceability to a standard time source.

5.4.2.5 Operation Mode Negotiation between CMTS Core and RPD

The CMTS Core initiates the operation mode negotiation with the RPD. The RPD MUST respond with its capability. CMTS Core determines which operation mode to use based on the RPD's and its own capabilities, then delivers the decision to the RPD. Refer to the [GCP] specification for details.

NOTE: Changing operation mode can be disruptive to the services.

5.5 Precision Timing Synchronization Services

5.5.1 Market Forces Drive Need for Precise Timing

In recent years, synchronization in access networks has become an important topic because of the evolution from time division multiplex (TDM)-based to packet-based networks. In particular, mobile wireless operators are struggling to increase their backhaul capacity that is required by the newest radio technologies. They are pushing themselves in order to provide greater bandwidth and improved services—things that are important to their customers.

Although the introduction of smaller capacity base stations (namely microcell, picocell, and femtocell) permits mobile and broadcast operators to improve wireless service by providing better coverage, it also requires increasing the number of network connections. Such trends lead to optimization of the mobile backhaul infrastructure. Various transmission options for the aggregation networks are being considered and/or utilized. As one of the last mile access transport technologies, the cable industry's hybrid fiber coax (HFC) networks are being considered, especially as the bandwidth of DOCSIS-based systems continues to increase.

One critical aspect of mobile base stations and broadcast transmitters is their need to synchronize their radio interfaces. Accurate frequency synchronization among base stations allows user handsets to seamlessly handover between base stations, reduces interference between cells, and optimizes radio bandwidth capacity. Another critical aspect of some base stations is the need for phase or ToD synchronization. In order to be utilized in the wireless market space, DOCSIS needs to support precision time synchronization.

5.5.2 DTP and R-DTI

The DOCSIS Timing Protocol (DTP) defined in DOCSIS MULPIv3.1 is a set of techniques coupled with extensions to the DOCSIS signaling messages. DTP allows the timing and frequency system of DOCSIS to be interfaced to external timing protocols such as PTP with high accuracy. The RPD MUST support DTP for the applications that require precision synchronization.

Supporting DTP alone is not adequate when the CMTS is divided into two entities: the CMTS Core and the RPD. In order to maintain the network traceability and high accuracy of the DTP, the R-DTI is defined to offer a highly accurate synchronization method between a precision time source and the network side interface (NSI) of the RPD.

5.5.3 Time Synchronization at NSI of RPD

5.5.3.1 Frequency Synchronization

As defined in [G.8261], two main classes of synchronization methods are identified in the Ethernet network, where the RPD is deployed with:

- Plesiochronous and network synchronous methods (i.e., a reference timing signal distributed over the synchronous physical layer). Synchronous Ethernet network is defined for this case.
- Packet-based methods. (PTP is one of the methods.)

Which methods are supported by the RPD node depends on the level of accuracy required by various applications.

5.5.3.1.1 Synchronous Ethernet

A Layer 1 frequency synchronization technique provides a higher level of frequency accuracy and stability, and as a result, a higher level of time accuracy becomes possible as well. Synchronous Ethernet is designed to deliver a physical layer clock through the network. A reference timing signal traceable to a PRC is injected into the Ethernet switch using an external clock port. This signal is extracted and processed via a synchronization function before injecting timing onto the Ethernet bit stream. The synchronization function provides filtering and may require holdover.

First defined in G.8261 (2006), then complemented by ITU-T G.8261 (2008), G.8262, G.8264 and a new release of G.781, Synchronous Ethernet specifies not only the method and requirements for frequency recovery and transmission, but also standardizes the advertisement of clock quality through the network. Like all Layer 1 frequency synchronization techniques, all network elements between network segments need to be capable of recovering and passing the frequency downstream. Therefore, changing a path from Ethernet to synchronous Ethernet requires all nodes in-line to be changed to use Ethernet equipment clock (EEC).

Synchronous Ethernet provides frequency traceability but not time information. Combined with IEEE 1588, and assuming careful planning and implementation, a very accurate time synchronization between two nodes across a packet network is achievable. When the frequency synchronization is implemented through synchronous Ethernet, and the phase/ToD synchronization is achieved through IEEE 1588, the EEC and 1588 GM share the same standard time source to avoid long-term frequency drift error.

5.5.3.1.2 Precision Time Protocol

PTP (see [IEEE 1588]) can be used to achieve frequency synchronization, as discussed in Section 5.3.4. ITU-T G.8261.1 specifies the hypothetical reference model (HRM) and the PDV network limits applicable when frequency synchronization is carried via packets and is recovered according to the adaptive clock recovery method as defined in Recommendations [G.8261] and [G.8260].

5.5.3.2 Phase/ToD Synchronization

While synchronous Ethernet only offers frequency traceability, The PTP (see [IEEE 1588]) can be used to achieve both frequency and phase synchronization as mentioned in Section 5.3.5. The 1588 Master Clock with a precision time source MAY be the CMTS Core or MAY be provided by other elements in the network. The devices between the master clock and RPD (slave clock) MAY be non-participant nodes, BCs, or TCs.

Non-participant nodes can introduce large amount of PDV that impacts the stability and/or the accuracy of the synchronization.

[IEEE 1588] boundary clocks (described in Section 5.3.2.2) can be used to divide the PDV effects into smaller segments and to increase the scale of 1588 deployments by distributing the burden of packet generation to multiple nodes within the network. Unfortunately, because boundary clocks are susceptible to the same error contributions as a slave node, they may actually have a negative impact on time alignment through the network. In between message updates, the boundary clock operates in holdover and therefore induces time and frequency error proportional to its onboard oscillator quality and slave servo algorithm.

Another type of PTP device is a transparent clock. It can be used in-line between a master port and slave port to provide PDV information to the slave. This technique enables an increase to the maximum number of nodes between a master and a slave with the same accuracy, or to increase the accuracy of time alignment between them with the same number of nodes. Because transparent clocks record the residency time of a packet, any error in timestamp location, frequency offset, or drift will have a negative impact on their performance.

Even with these techniques, achieving highly accurate results with IEEE 1588 requires very careful planning and implementation.

5.5.3.3 Deployment Scenarios

In a CMTS Core + RPD system, the synchronization performance of the RPD becomes the key element to the overall DTP performance. Although a CMTS Core can participate as a 1588 GM or BC, the RPD may receive another and possibly better clock source within the network.

Some deployment examples are shown in Figure 12, Figure 13, Figure 14, and Figure 15.

5.5.3.3.1 Scenario 1

Figure 12 shows a deployment with these elements: CMTS Core is a 1588 OC Grandmaster, the RPD is a 1588 OC slave, and there are an indefinite number of non-participant nodes in between. The non-participant nodes are shown in white.

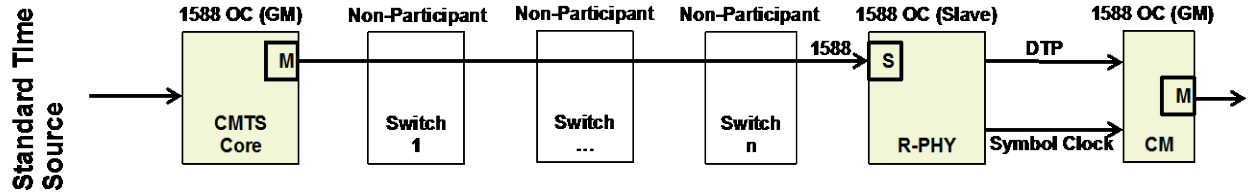

Figure 12 - Network Deployment Example 1

5.5.3.3.2 Scenario 2

Figure 13 shows a deployment with these elements: CMTS Core is a 1588 BC, the RPD is a 1588 OC slave, there are an indefinite number of BC nodes in between, and all nodes are Synchronous Ethernet capable.

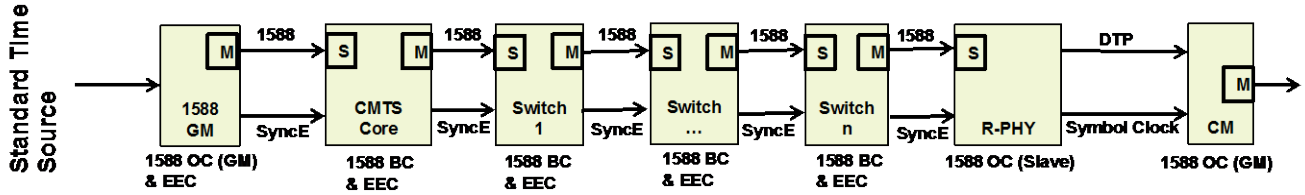

Figure 13 - Network Deployment Example 2

5.5.3.3.3 Scenario 3

Figure 14 shows a deployment with these elements: External Node is a 1588 OC Grandmaster, the RPD is a 1588 OC slave, the CMTS Core is a 1588 OC slave, and there are an indefinite (and mixed) number of node types in between. The non-participant nodes are shown in white.

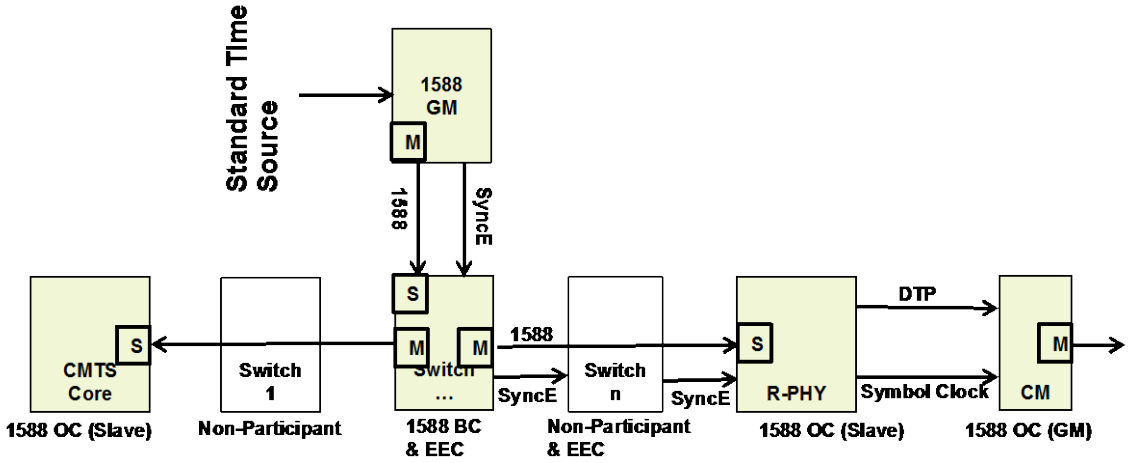

Figure 14 - Network Deployment Example 3

5.5.3.3.4 Scenario 4

In the example shown in Figure 15, the RPD synchronizes to a 1588 GM while the Node_Master is implemented for DOCSIS operation between the CMTS Core and the RPD. The External Node is a 1588 OC grandmaster, the RPD is a 1588 BC, and the CMTS Core is a 1588 OC slave. The physical clock of CMTS Core may be a different 1588 clock domain.

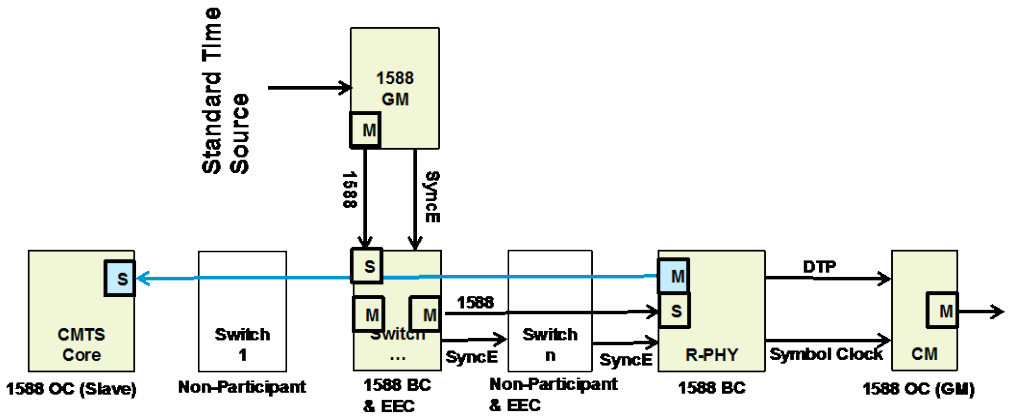

Figure 15 - Network Deployment Example 4

5.5.3.4 Timing Requirements Consideration

The performance requirements of the frequency and/or phase synchronization are driven by the application. It is important to recognize that the R-DTI only covers the synchronization between the RPD and the standard time reference over the NSI. It is only one part of the DTP system. The timing error between the RPD to the standard time source can be categorized similarly as the error source defined in the "DTP System Level Performance" section of [MULPIv3.1].

5.6 MPEG-TS Video

For Moving Picture Experts Group transport stream (MPEG-TS) video services, the RPD receives only constant bit rate (CBR) multi program transport streams (MPTSs), and manages frequency drift between the CCAP-Core and the RPD independent of R-DTI. The RPD MUST have an MPEG compliant clock.

5.7 NDF and NDR Synchronization[6]

5.7.1 NDF

The Remote PHY narrowband digital forward (NDF) refers to the digitizing of an analog portion of the downstream spectrum at the headend, sending the digital samples as payload in DEPI packets to the RPD, and then re-creating the original analog stream at the Remote PHY.

Since the RPD plays out the samples into a digital-to-analog converter as a continuous stream of samples, the samples provided by the CCAP-Core cannot overflow or underrun the FIFO buffer in the Remote PHY. For this reason, the CCAP-Core and the RPD MUST remain frequency locked.

5.7.2 NDR

The Remote PHY narrowband digital return (NDR) refers to the digitizing of an analog portion of the upstream spectrum at the RPD, sending the digital samples as payload in upstream external PHY interface (UEPI) packets to the CCAP-Core, and then re-creating the original analog stream at the headend.

Since the headend plays out the digital samples at fixed rate, the rate of samples received from the RPD needs to match the CCAP-Core rate such that the FIFO buffers in the CCAP-Cores do not overflow or underrun. For this reason, the CCAP-Core and the RPD MUST remain frequency locked.

[6] Revised per R-DTI-N-15.1361.3 on 9/20/15 by JB.

6 SYSTEM TIMING REQUIREMENTS[7]

The requirements in this section are independent of the synchronization methods or operation modes described in Section 5.

6.1 DOCSIS Timing Requirements

6.1.1 RPD Master Clock Frequency Accuracy for DOCSIS

The 10.24 MHz RPD master clock MUST meet the frequency accuracy requirement specified in section 6.3.5.2 of [DRFI], over a temperature range of 0 to 40 (TBD) degrees C and for up to ten (TBD) years from date of manufacture.

6.1.2 RPD Master Clock Jitter

The 10.24 MHz RPD master clock MUST meet the double sideband phase noise requirements over the specified frequency ranges defined in CMTS or EQAM Master Clock Jitter for Synchronous Operation, section 6.3.5.3 of [DRFI], and DTI Client Test Port Clock, section 7.2.7 of [DTI]. The requirements are summarized in Table 2.

Table 2 - RPD 10.24 MHz Master Clock Double Sideband Phase Noise Requirements

	Double Sideband Phase Noise Requirements	Jitter
10 Hz to 100 Hz	<-53 dBc	<0.035 ns RMS
100 Hz to 1 kHz	<-61 dBc	<0.014 ns RMS
1 kHz to 10 kHz	<-53 dBc	<0.035 ns RMS
10 kHz to 5.12 MHz	<-53 dBc	<0.035 ns RMS

6.1.2.1 RPD Master Clock Frequency Drift

The frequency of the RPD master clock MUST meet the drift requirement specified in CMTS or EQAM Master Clock Jitter for Asynchronous Operation, section 6.3.5.2 of [DRFI].

6.1.2.2 RPD Clock Generation

Section 6.1.3 contains the RPD requirements for locking the downstream symbol clock to the master clock.

6.1.2.3 RPD Clock Generation for DOCSIS 3.0

The RPD MUST lock the downstream symbol clock to the RPD master clock using the M/N divisor specified in CMTS Clock Generation, section 6.3.6.1 of [DRFI].

6.1.2.4 Downstream Symbol Rate

See Downstream Symbol Rate, section 6.3.6.3 of [DRFI].

6.1.2.5 Downstream Symbol Clock Jitter for Synchronous Operation

See Downstream Symbol Rate for Downstream Symbol Clock Jitter for Synchronous Operation, section 6.3.7 of [DRFI].

6.1.2.6 Downstream Symbol Clock Drift for Synchronous Operation

See Downstream Symbol Clock Drift for Synchronous Operation, section 6.3.8 of [DRFI].

[7] Revised per R-DTI-N-15.1361.3 on 9/20/15 by JB.

6.1.2.7 Timestamp Jitter

The DOCSIS timestamp jitter at RPD MUST meet the timestamp jitter requirement specified in section 6.3.9, the Timestamp Jitter section of [DRFI], that is, be less than 500 ns peak-to-peak at the output of the downstream transmission convergence sublayer. This jitter is relative to an ideal downstream transmission convergence sublayer that transfers the MPEG packet data to the downstream physical media dependent sublayer with a perfectly continuous and smooth clock at the MPEG packet data rate. Downstream physical media dependent sublayer processing MUST NOT be considered in timestamp generation and transfer to the downstream physical media dependent sublayer.

Thus, any two timestamps N1 and N2 (N2 > N1) which were transferred to the downstream physical media dependent sublayer at times T1 and T2 respectively MUST satisfy the following relationship:

$$|((N2 - N1))/f_{RPD} - (T2 - T1)| < 500 \times 10^{-9}$$

In the equation, the value of (N2-N1) is assumed to account for the effect of rollover of the timebase counter, and T1 and T2 represent time measured in seconds. f_{RPD} is the actual frequency of the RPD master timebase and may include a fixed frequency offset from the nominal frequency of 10.24 MHz. This frequency offset is bounded by a requirement stated farther below in this section.

The jitter includes inaccuracy in timestamp value and the jitter in all clocks. The 500 ns allocated for jitter at the downstream transmission convergence sublayer output MUST be reduced by any jitter that is introduced by the downstream physical media dependent sublayer.

NOTE: Jitter is the error (i.e., measured) relative to the RPD local clock.

6.1.3 RPD Clock Generation for DOCSIS 3.1

This section specifies the timing and frequency synchronization requirements for DOCSIS 3.1 RPD transmitters.

The purpose of this section is to ensure that the RPD transmitter can provide proper timing and frequency references for DOCSIS 3.1 downstream orthogonal frequency division multiplexing (OFDM) operation.

The RPD downstream OFDM symbol and subcarrier frequency and timing relationship is defined in section 7.3.3, the Subcarrier Clocking section of [PHYv3.1].

6.1.3.1 Downstream Sampling Rate

The RPD MUST lock the 204.8 MHz downstream OFDM Clock to the 10.24 MHz RPD Master Clock specified in section 7.5.3.1, the Downstream Sampling Rate section of [PHYv3.1].

6.1.3.2 Downstream OFDM Symbol Clock Jitter

The RPD MUST adhere to the following double sideband phase noise requirements for the downstream OFDM symbol clock over the specified frequency ranges specified in section 7.5.3.3, the Downstream OFDM Symbol Clock Jitter section of [PHYv3.1].

6.2 MPEG-TS Video

The system timing clock (STC) at the RPD MUST meet the frequency accuracy requirement (≤ ±30 PPM) and the drift requirement (≤ 10 PPM/hour) specified by [ISO 13818-1].

6.3 Video OOB

This section specifies the timing and frequency synchronization requirements for the video OOB frequency.

6.3.1 OOB 55-1

The RPD master clock MUST meet the frequency accuracy and stability requirements (≤ ±100 PPM) specified by [SCTE 55-1].

6.3.2 OOB 55-2

The RPD master clock MUST meet the frequency accuracy and stability requirements (≤ ±50 PPM) specified by [SCTE 55-2].

7 R-DTI IMPLEMENTATION SPECIFIC REQUIREMENTS

7.1 Protocol Support

CCAP-Core MUST support PTP messages over the following encapsulations defined in [IEEE 1588]:

- PTP over Ethernet/IEEE 802.3
- PTP over UDP over IPv4
- PTP over UDP over IPv6

RPD MUST support PTP messages over the following encapsulations defined in [IEEE 1588]:

- PTP over Ethernet/IEEE802.3
- PTP over UDP over IPv4
- PTP over UDP over IPv6

CCAP-Core MUST support the unicast model defined in [IEEE 1588].

RPD MUST support the unicast model defined in [IEEE 1588].

7.2 DOCSIS Timing Requirements

The RPD MUST support Node_Slave mode:

- RPD MUST support 1588 OC slave.
- RPD MUST meet all requirements specified in Section 6.1 and subsections thereof.
- RPD MUST meet time/phase synchronization accuracy of ± 1 ms in reference to the 1588 GM.
- RPD MUST inject the DOCSIS timestamp derived from the 1588 domain into the DOCSIS downstream path.
- RPD MUST use the DOCSIS timestamp derived from the 1588 domain to receive packets on an upstream receiver interface.

The CMTS Core MUST support Node_Slave mode:

- CMTS Core MUST support 1588 OC grandmaster.
- When CMTS Core operates as 1588 OC grandmaster, CMTS Core clock MUST meet the frequency accuracy and stability requirements specified in DRFI Output Electrical, section 6.3.5 of [DRFI].
- CMTS Core MUST support 1588 OC slave.
- When CMTS Core operates as 1588 slave, CMTS Core MUST meet the time/phase synchronization accuracy of ± 1 ms in reference to the 1588 GM.
- CMTS Core MAY support 1588 BC.

The RPD MUST support Node_Master mode:

- RPD MUST support 1588 OC grandmaster.
- RPD MAY support 1588 BC.
- RPD MUST meet all requirements specified in Section 6.1 and subsections thereof.
- RPD MUST inject the local timestamp into the DOCSIS downstream path.
- RPD MUST use the same local DOCSIS timestamp to receive packets on an upstream receiver interface.

CMTS Core SHOULD support Node_Master mode. When CMTS Core operates in Node_Master mode:

- CMTS Core MUST support 1588 OC slaves to multiple 1588 clock domains.

- CMTS Core MUST generate MAPs based on the DOCSIS timestamps of the individual 1588 clock domains which are owned by individual RPDs.
- Time/phase synchronization between the RPD and the CMTS Core MUST be within ± 1 msec.

7.3 Precision Timing Services

The RPD and the CCAP-Core MUST support the following timing requirements:

- RPD MUST support DTP.
- RPD MUST support 1588 OC slave.
- RPD SHOULD support Synchronous Ethernet.
- RPD MAY support 1588 BC.
- CCAP-Core MAY support 1588 OC grandmaster.
- CCAP-Core MAY support Synchronous Ethernet.
- CCAP-Core MAY support 1588 BC.

7.3.1 Frequency Synchronization

The frequency synchronization performance of R-DTI is characterized by the frequency accuracy and can be categorized as shown in Table 3.

Table 3 - R-DTI Frequency Synchronization Performance

	Level I System	Level II System	Level III System	Level IV System	Level V System
f-rdti	± 5 PPB	± 16 PPB	± 50 PPB	± 100 PPB	± 250 PPB

7.3.2 Phase/Time Synchronization

The phase/time synchronization performance of R-DTI is characterized by the timing error between the standard time source and RPD, and can be categorized as shown in Table 4.

Table 4 - R-DTI Phase Synchronization Performance

	Level I System	Level II System	Level III System	Level IV System	Level V System
T-rdti-error	± 20 ns	± 40 ns	± 100 ns	± 200 ns	± 500 ns

7.4 NDF and NDR

The RPD and the CCAP-Core MUST support the following NDF and NDR requirements:

- CCAP-Core MUST support [IEEE 1588] OC grandmaster.
- CCAP-Core Master Clock MUST meet the frequency accuracy and stability spec defined in the DRFI Output Electrical section of [DRFI].
- RPD MUST support [IEEE 1588] OC slave.
- RPD MUST meet all the requirements specified in section 6 and subsections thereof.
- RPD MAY support Synchronous Ethernet.
- The MTIE (Maximum Time Interval Error) of the RPD clock is a reference to the CCAP-Core clock. The MTIE MUST be less than 1 ms in any given observation interval.

Appendix I RPD and DOCSIS System Performance

I.1 Introduction

Compared to an I-CMTS system, inserting a CIN between the CCAP-Core and the RPD increases the round-trip time of the DOCSIS system, and may impact system performance.

I.2 Round-Trip Time and Performance

Broadly speaking, round-trip time is the time from a CM's request to the time the CM transmits the data that corresponds to that request. The more quickly all this happens, the sooner the CM can transmit another request (for example, a piggyback request), thereby transmitting more data, etc.

Round-trip time limits the performance of a single modem by limiting the number of grants the modem can receive in a given time. For instance, if the system round-trip time is 10 ms, it is not possible for a modem to receive more than 100 grants per second. If every grant were the size of the modem's allowed maximum burst size (as configured by, e.g., Maximum Concatenated Burst, [RFIv2.0]), an upper bound on the modem's performance could be found by the following simple calculation:

max throughput (bits/sec) = max burst (bits) × 1/ [round trip time (sec)]

In practice, due to the need to share bandwidth among many users and services, the maximum burst size needs to be limited to reasonable values, and the CCAP-Core generally cannot grant the maximum burst size in every grant, even if a modem requests it.

A longer round-trip time also increases the access latency seen by a single modem, that is to say, the time it takes for a modem to gain access to the upstream to begin transmission of new data after an idle period. Conversely, if reducing round-trip time enables higher throughput to be achieved or speeds the opening of the TCP window, the modem's transactions (e.g., download of an FTP file or HTTP web page) may be completed more quickly (assuming plant bandwidth is available to use). These factors may in turn affect the overall bandwidth efficiency of the system.

In DOCSIS 3.0 mode, the CM is able to send more requests before the grants. This reduces the round-trip time impact to the performance.

I.3 Elements of Round-Trip Time

It is convenient to begin measurement of round-trip time at the instant when a modem begins transmission of a request. Round-trip time can then be measured as the time from this initial request to the instant when the modem begins transmission of its next request. These events can be easily captured on a network sniffer.

The elements of round-trip time may be categorized as follows:

- *Upstream propagation delay*: time occupied by plant delays in the upstream direction.
- *Upstream reception and request parsing time*: time from the start of burst arrival at the RPD until the reception and parsing of the request to MAC-layer is complete. This includes the upstream PHY processing time; encapsulation of the request into a UEPI packet; queueing and transmission of the UEPI packet at the egress of the RPD; delay and jitter of the CIN; queueing, and processing delays inside the CMTS Core.
- *Scheduler queuing and processing delay*: time from arrival of the request at the scheduler until completion of the MAP message containing a grant for the request. If the request arrives just after the scheduler has finished creating a MAP, the request is delayed by the time interval until the next MAP. On the other hand, if the request arrives just before the scheduler finishes creating a MAP, the request may see nearly zero delay. In general, the actual queuing delay is a random variable between zero and the maximum MAP interval.

  Under some lab conditions involving only one or a few CMs, this delay may appear to be constant, but this cannot generally be assumed in a real system. Some scheduler implementations may vary the MAP interval to optimize this delay. The time required for the scheduler to make scheduling decisions and actually create the MAP message is also included here. This factor is implementation-dependent.

- *MAP delivery time (to the* RPD *DOCSIS PHY layer)*: The time from the completion of the MAP message creation, to delivery of the MAP to the PHY layer. This includes any time consumed by the CMTS Core's MAC function; encapsulation of the MAP into a DEPI packet; queuing and transmission of the DEPI packet at the egress of the CMTS Core; delay and jitter of the CIN; queuing and processing delays inside the RPD; and any delay in inserting the MAP into the MPEG-encapsulated DOCSIS stream (e.g., due to the need to wait for a previous packet to complete transmission).
- *Downstream physical-layer delays*: This includes the latency of the downstream modulator, downstream interleaver delay, and physical propagation delay between the RPD and the CM.
- *CM MAP processing time*: The time from arrival of the first bit of the MAP at the CM, until the MAP becomes effective. The minimum value is specified in the Relative Processing Delay section of [RFIv2.0]. It accounts for all internal CM processing delays.
- *Time until grant*: If the first grant in the MAP is not available to this CM, the CM's actual transmission will be "delayed" until the actual time of the grant.
- *Margin*: In practice, the CMTS Core cannot precisely control all delays to guarantee that MAPs arrive at the modem at exactly the right instant. Thus, the CMTS Core needs to add margin to account for worst-case propagation delays to the farthest modems, variations in MAP creation time, and CIN delays.

Table 5 lists sample values for the round-trip time components described above. These values are given ONLY by way of example and should not be interpreted as typical values applying to any particular system.

Table 5 - Sample Values for the Round-Trip Time Components

Delay Source	Subtotal	Total	Remarks
Upstream propagation time		800	
Physical HFC plant delay	800		Approx. 100 miles
Upstream reception/parsing time		852 + CIN_{us}	
Upstream PHY processing time	369		Time for 1 FEC block (236,200) at 5.12 Mbps
UEPI packetization at RPD	383		
RPD to CMTS Core CIN Delay	varies		
Upstream MAC processing time	100		
Scheduler queuing and processing	1000	1000	
MAP delivery to PHY layer		1338 + CIN_{ds}	
DEPI packetization at Core	383		For MPT mode, transmit time of 7 MPEG packets
CMTS Core to RPD CIN Delay	varies		
RPD latency	500		Per [R-PHY] specification
Queuing behind max-length packet MPEG encaps	455		Packet size of 1518 bytes (64-QAM)
Downstream transmission line		1841	
MAP duration on wire	61		200B MAP at 64-QAM
Downstream FEC/interleaver delay	980		(I, J) = (32, 4) at 64-QAM
Downstream propagation limit	800		Approx. 100 miles
MAP advance margin		1500	Includes 1 ms budget for synchronization error
CM processing time		200	TDMA, no byte interleaving
		7531 + (CIN_{us} + CIN_{ds})	

In Table 5, factors shown in italics need to be considered in the MAP advance calculation.

Appendix II Acknowledgements

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Contributor	Company Affiliation
John T. Chapman	Cisco
Hang Jin	Cisco
Pawel Sowinski	Cisco
Yi Tang	Cisco

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Contributor	Company Affiliation	Contributor	Company Affiliation
Bill Powell	Alcatel-Lucent	Nagesh Nandiraju	Comcast
Brian Kurtz	Altera	Saifur Rahman	Comcast
Carlton Lane	Analog	Jorge Salinger	Comcast
Linda Mazaheri	Analog	Joe Solomon	Comcast
Tom Ferreira	Arris	Douglas Will	Comcast
Steve Foley	Arris	Jeff Ford	Complex IQ
Anand Goenka	Arris	Al Garrett	Complex IQ
Jeff Howe	Arris	Ony Anglade	Cox Communications
Hari Nair	Arris	Mike Cooper	Cox Communications
Andrew Chagnon	Broadcom	Samir Parikh	Gainspeed Networks
Victor Hou	Broadcom	João Campos	Get
Niki Pantelias	Broadcom	Even Kristoffersen	Get
David Pullen	Broadcom	Adi Bonen	Harmonic
Stuart Hoggan	CableLabs	Mike Patrick	Harmonic
Volker Leisse	CableLabs	Jim Chen	Huawei
Karthik Sundaresan	CableLabs	Hesham ElBakoury	Huawei
Nikhil Tayal	CableLabs	Karl Moerder	Huawei
Jun Tian	CableLabs	Jack Moran	Huawei
Andrew Sundelin	CableLabs Consultant	Guangsheng Wu	Huawei
Naor Goldman	Capacicom	Phil Oakley	LGI
Dave Fox	Casa Systems	Stan Bochenek	Maxim Integrated
Maike Geng	Casa Systems	Ajay Kuckreja	Maxim Integrated
David Claussen	Charter	Len Dauphinee	MaxLinear
Nobo Akiya	Cisco	David Huang	MaxLinear
Alon Bernstein	Cisco	Louis Park	MaxLinear
Brian Bresnahan	Cisco	Sridhar Ramesh	MaxLinear
John T. Chapman	Cisco	Patrick Tierney	MaxLinear
Hang Jin	Cisco	Scott Walley	MaxLinear
Tong Liu	Cisco	Rei Brockett	Pace/Aurora

Contributor	Company Affiliation	Contributor	Company Affiliation
Carlos Pignataro	Cisco	Nasir Ansari	Rogers
Sangeeta Ramakrishnan	Cisco	George Hart	Rogers
John Ritchie	Cisco	Kevin Kwasny	Shaw
Pawel Sowinski	Cisco	Lee Johnson	ST Micro
Don Strausberger	Cisco	Paul Brooks	Time Warner Cable
Yi Tang	Cisco	Kirk Erichsen	Time Warner Cable
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Appendix III Revision History

III.1 Engineering Change for CM-SP-R-DTI-I02-151001

ECN	Date Accepted	Summary	Author
R-DTI-N-15.1361-3	09/09/2015	Restructuring of DTI specification	Dave Fox